REMARKS

Claims 1-18 are pending. Claims 11-18 have been withdrawn from examination. Claims 1, 7 and 8 stand rejected under 35 U.S.C. §102(b) as being unpatentable over Ninomiya (US 5,617,359). Claim 10 stands rejected under 35 U.S.C. 102(b) as being unpatentable over Shin (US 6,076,138). Claim 9 stands rejected under 35 U.S.C. 103(a) as being obvious over Shin in light of Satoh (US 6,493,265). In response thereto, applicants respectfully submit the following remarks.

Applicants' Response to Claim Rejections under 35 U.S.C. § 102(b)

Claims 1, 7 and 8 stand rejected under 35 U.S.C. 102(b) as being anticipated by Ninomiya U.S. Patent No. 5,617,359. In Figure 6 of Ninomiya, the Office Action interpretes ST11, wherein the source line is compared to Vref, as equivalent to the first pass/fail decision process of claim 1. If the source line fails ("No") than the erase voltage is maintained. See col. 9, lines 45-49. The Office Action holds this equivalent to "applying a signal to the memory cell ... to charge an amount of change stored..." in claim 1. The Office action holds that the second decision of claim 1 is equivalent to phase II of Ninomiya.

Applicants respectfully submit that not all the limitations of claim 1 are disclosed in Ninomiya. Specifically, the relation of the relaxation and the severity in the first and second deciding conditions of Ninomiya is opposite to that in the first and second deciding conditions of claim 1. Therefore, Ninomiya does not disclose the limitation "a second deciding condition that is relaxed rather than the first deciding condition."

In the nonvolatile semiconductor memory of claim 1, the first decision process and the second decision process are executed. In the case of the erase verification, for example, in the first decision process, the pass/final of the data read from the memory cell are decided by the first deciding condition. The erase pulse (the signal) is applied to the memory that is decided as fail to change an amount of charge stored in the memory cell. Then, in the second decision process, the pass/fail of the data read from the memory cell are decided by the second deciding condition that is relaxed rather than the first deciding condition. In this manner, the second deciding condition is relaxed rather than the first deciding condition, that is, the first deciding condition is severe rather than the second deciding condition.

On the other hand, the EEPROM of Ninomiya, shown in Fig. 6 - Fig. 8, the first phase and the second phase constituting the erase operation are executed. In the first phase, the potential level on the source line VS is monitored, the erasing signal is maintained to apply to the source line VS until the source line VS reaches the reference level Vref. When the potential level on the source line VS has reached the reference level Vref, the erasing signal is turned off. In other words, in the first phase, the erasing to the memory cell is maintained to execute until the threshold of the memory cell reaches a state close to the appropriate erased state. Then, in the second phase, the threshold of the memory cell reaches the appropriate erased state by repeating the verification and the erasing.

In Ninomiya, the pass/fail are decided by whether the threshold of the memory cell has reached a state close to the appropriate erased state or not in the first phase, and the pass/fail are decided by whether the threshold of the memory cell has reached the appropriate erased state or not in the second phase. Thus, the deciding condition of the first phase is relaxed rather than the deciding condition of the second phase.

In claim 1, since the pass/fail are decided by the first deciding condition that is severe rather than the second deciding condition in the first decision process, it is possible to detect the memory cell that has such a possibility that its pass/fail decision become unreliable because of the influence of the noise in the second decision process. And, since the erase pulse (the signal) is applied to such memory cell to change an amount of charge stored, it is possible to strengthen the erased state (the data) of such memory cell. Thus, in the second decision process that must be decided as pass finally, it is decided as pass almost certainly by one pass/fail decision.

On the other hand, in Ninomiya, since the pass/fail are decided by the first deciding condition that is relaxed rather than the second deciding condition in the first phase, it is impossible to detect the memory cell that has such a possibility that its pass/fail decision is unreliable because of the influence of the noise in the second phase and to strengthen the erased state of such memory cell. Thus, in the second phase that must be decided as pass finally, it is hardly decided as pass by one pass/fail decision, and it is necessary to execute two or more pass/fail decision (see in column 11, lines 9-13 of Ninomiya). Therefore, the relation of the relaxation and the severity in the first and second deciding conditions of Ninomiya is opposite to that in the first and second deciding conditions of claim 1. Applicants respectfully submit that the rejection to claims 7 and 8 are likewise addressed by nature of their dependency on claim 1.

Claim 10 stands rejected under 35 U.SC. 102(b) as being anticipated by Shin U.S. Patent No. 6,076,138. The nonvolatile semiconductor memory operating method of claim 10 includes the first decision process and the second process. Applicants respectfully submit that the first and second decision processes of claim 10 are the same operation as those of claim 1 discussed above.

On the other hand, the flash memory operating method (pre-programming method) of Shin, shown in FIG. 5, includes the decision process of steps 203-208 and the decision process of steps 209-217. In the decision process of steps 203-208, the programming is executed (step 204), and the verification to detective counters is performed (step 205). Then in decision process of steps 209-217, the verification is performed to determine whether the cell is normally programmed or not (step 210).

However, Shin does not teach or suggest the relation of the relaxation and the severity in the deciding condition of steps 203-208 and that of steps 209-217. And, in the decision process of steps 203-209, when it has been verified a detective counter at the verification of step 205 (when it has been decided as fail at the verification of step 205), the pumping-down for the verification of step 210 is performed (step 208), but an amount of charge stored in cell is not changed.

Thus, in Shin, it is impossible to detect the cell that has such a possibility that its pass/fail decision become unreliable in the verification of step 210 because of the influence of the noise and to strengthen the data of such cell. Therefore, in the verification of step 210 that must be decided as pass finally, it is not certainly to be decided as pass by one pass/fail decision. Wherefore, in light of the above, applicants respectfully request favorable reconsideration.

Applicants' Response to Claim Rejections under 35 U.S.C. § 103(a)

Claim 9 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Shin U.S. Patent (USP) No. 6,076,138 in view of Satoh et al. U.S. Patent 6,493,265. Claim 9 depends from claim 1. Thus, in claim 9, as in claim 1, since the pass/fail are decided by the first deciding condition that is severe rather than the second deciding condition in the first decision process, it

is possible to detect the memory cell that has such a possibility that its pass/fail decision is unreliable because of the influence of the noise in the second decision process. And, since the signal (e.g. the erase pulse) is applied to such memory cell to change an amount of charge stored, it is possible to strengthen the data (e.g. the erased state) of such memory cell. Therefore, also in claim 9, in the second decision process that must be decided as pass finally, it is decided as pass almost certainly by one pass/fail decision. Applicants respectfully submit that neither of the cited references discloses this limitation.

As described above, Shin does not teach or suggest the relation of the relaxation and the severity in the deciding condition of steps 203-208 and that of steps 209-217. And, in Shin, when it has been decided as fail at the verification of step 205, an amount of charge stored in the cell is not changed in the decision process of steps 203-208. Thus, in Shin, in the verification of step 210 that must be decided as pass finally, it is not certainly to be decided as pass one pass/fail decision.

Moreover, in claim 9, the first deciding condition and the second deciding condition, that is, two deciding conditions are set individually every level. On the other hand, in Satoh, shown in FIG. 20B, for example, read voltages Vtc1, Vtc2 and Vtc3 that are different from each other, are used as deciding condition in the case that four data "00", "01" or "10" and "11" are decided. Either "11" or "00", "01" and "10" is decided by Vtc1, and either "10" or "00" and "01" is decided by Vtc2 and either "01" or "00" is decided by Vtc3. In short, in Satoh, one deciding condition (Vtc1, Vtc2 or Vtc3) is set individually every level. In this manner, the number of deciding condition set individually every level of Satoh is different from that of claim 9. Hence, the combination of the references would not result in the presently claimed invention. Wherefore, applicants respectfully request favorable reconsideration.

In view of the aforementioned accompanying remarks, Applicants submit that that the claims are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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